

WHAT IS CLAIMED IS:

1. A semiconductor die comprising a first crystallized silicon layer, said first crystallized silicon layer comprising a first area bounded by four adjacent nucleation sites, said first area having no more than five crystal grain boundaries and said first area having no amorphous silicon.
2. The die of claim 1, further comprising a plurality of thin film transistors formed in the crystallized silicon layer.
3. The die of claim 2 wherein the thin film transistors are memory cells.
4. The die of claim 3, further comprising a monolithic three dimensional memory array.
5. The die of claim 1, wherein the nucleation sites are created by depositing silicon nuclei.
6. The die of claim 1, wherein the nucleation sites are created by depositing germanium.
7. A method for crystallizing a polysilicon layer on a wafer, the method comprising:
forming a first amorphous silicon layer;
selectively introducing a crystallizing agent on the amorphous layer in a
substantially symmetric pattern in two dimensions; and
annealing the wafer to form the crystallized polysilicon layer, wherein
substantially no amorphous silicon remains between silicon grains in the
polysilicon layer.
8. The method of claim 7 wherein the crystallizing agent is silicon nuclei.
9. The method of claim 8 wherein the step of selectively introducing a crystallizing agent in a substantially symmetric pattern comprises:

- forming a mask layer on the first amorphous silicon layer;
etching holes in the mask layer, the holes distributed in a substantially symmetric pattern and exposing portions of the first amorphous layer; and
depositing silicon nuclei on the mask layer and the exposed portions of the first amorphous layer.
10. The method of claim 9 further comprising, before the annealing step, forming a second layer of amorphous silicon on and in contact with the first amorphous silicon layer and the silicon nuclei.
11. The method of claim 7 wherein the crystallizing agent is germanium.
12. The method of claim 11 wherein the step of selectively introducing a crystallizing agent in a substantially symmetric pattern comprises:
forming a mask layer on the first amorphous silicon layer;
etching holes in the mask layer, the holes distributed in a substantially symmetric pattern in two dimensions and exposing portions of the first amorphous layer;
and
depositing germanium on the mask layer and the exposed portions of the first amorphous layer.
13. The method of claim 12 further comprising, before the annealing step, forming a second layer of amorphous silicon on and in contact with the first amorphous silicon layer and the germanium.
14. The method of claim 7 wherein the crystallizing agent is laser energy.
15. The method of claim 14 wherein the step of selectively introducing a crystallizing agent in a substantially symmetric pattern comprises treating the first amorphous layer with a laser at locations distributed in a substantially symmetric pattern.

16. The method of claim 15 wherein the step of selectively introducing a crystallizing agent in a substantially symmetric pattern comprises creating a laser interference pattern, and wherein a plurality of thin film transistors is formed, channel regions of the thin film transistors formed in the polysilicon layer.
17. The method of claim 7 wherein a plurality of thin film transistors is formed having channel regions formed in the polysilicon layer.
18. The method of claim 17 wherein the thin film transistors are memory cells.
19. The method of claim 18 wherein the memory cells are SONOS devices.
20. The method of claim 18 wherein the memory cells are floating gate devices.
21. The method of claim 18 wherein the memory cells are a portion of a memory level in a monolithic three dimensional memory array.
22. A method for producing a wafer having a crystallized silicon layer with controlled defect density, the method comprising:
 - forming a first layer of amorphous silicon on the wafer;
 - selectively introducing a crystallizing agent on the amorphous silicon layer in a substantially symmetric pattern across a seeded area; and
 - annealing the amorphous silicon layer, wherein, after the annealing step, in the seeded area, an area bounded by adjacent nucleation sites encloses no more than five crystal grain boundaries.
23. The method of claim 22 wherein the symmetric pattern is substantially evenly spaced in two dimensions.
24. The method of claim 22 wherein the crystallizing agent is silicon nuclei.

25. The method of claim 24 further comprising, before the annealing step, forming a second layer of amorphous silicon on and in contact with at least portions of the first amorphous silicon layer.
26. The method of claim 24 wherein the crystallizing agent is germanium.
27. The method of claim 26 further comprising, before the annealing step, forming a second layer of amorphous silicon on and in contact with at least portions of the first amorphous silicon layer.
28. The method of claim 22 wherein the crystallizing agent is laser energy.
29. The method of claim 22 wherein a monolithic three dimensional memory array comprising charge storage devices is fabricated on the wafer, portions of the devices comprising portions of the crystallized silicon layer.
30. A method for controlling grain uniformity on a wafer, the method comprising:
 forming a first layer of amorphous silicon on the wafer;
 selectively introducing a crystallizing agent at substantially uniform intervals across an area of the amorphous silicon layer;
 forming a second layer of amorphous silicon on and in contact with at least portions of the first layer of amorphous silicon; and
 annealing the wafer to convert the amorphous silicon layers to a polysilicon layer.
31. The method of claim 30 wherein the crystallizing agent is silicon nuclei.
32. The method of claim 30 wherein the crystallizing agent is germanium.
33. The method of claim 30 wherein the crystallizing agent is laser energy.

34. The method of claim 30 wherein the uniform intervals are substantially evenly spaced in two dimensions.
35. The method of claim 30 wherein a plurality of thin film transistors is formed, having channel regions formed in the polysilicon layer.
36. The method of claim 35 wherein the plurality of thin film transistors form a portion of a monolithic three dimensional memory array.
37. A method for maximizing grain size and controlling density of grain boundaries in crystallized silicon, the method comprising:
- forming a first amorphous silicon layer on a wafer;
 - selectively creating nucleation sites at substantially uniform intervals on the first amorphous silicon layer;
 - annealing the wafer to convert the amorphous layer to polysilicon; and
 - forming a plurality of memory cells in the polysilicon, wherein portions of the cells comprise portions of the polysilicon, and wherein placement of the nucleation sites and placement of individual memory cells is not coordinated.
38. The method of claim 37 wherein the uniform intervals are substantially evenly spaced in two dimensions.
39. The method of claim 37 wherein the step of selectively creating nucleation sites at uniform intervals comprises depositing silicon nuclei.
40. The method of claim 37 wherein the step of selectively creating nucleation sites at uniform intervals comprises depositing germanium.
41. The method of claim 37 wherein the step of selectively creating nucleation sites at uniform intervals comprises exposing the first amorphous silicon layer to laser energy at uniform intervals.

42. The method of claim 37 wherein the plurality of memory cells is a portion of a monolithic three dimensional memory array.
43. A method for maximizing grain size and controlling density of grain boundaries in silicon, the method comprising:
- forming a first amorphous silicon layer on a wafer;
 - selectively creating nucleation sites at uniform intervals on the amorphous silicon layer;
 - annealing the wafer to form polysilicon wherein substantially no amorphous silicon remains between silicon grains; and
 - forming a plurality of active devices, the devices at least partially formed in the polysilicon.
44. A method for controlling grain boundaries in a polysilicon layer, the method comprising:
- forming a first amorphous silicon layer on a wafer;
 - forming a mask layer having holes at substantially uniform intervals on and in contact with the first amorphous silicon layer wherein the amorphous silicon layer is exposed in the holes;
 - depositing a crystallizing agent on the mask layer and on the first amorphous silicon layer;
 - forming a second amorphous silicon layer in contact with at least portions of the first amorphous silicon layer, and
 - annealing the wafer.
45. The method of claim 44 wherein the holes are substantially evenly distributed in two dimensions.
46. The method of claim 44 wherein the crystallizing agent is germanium.

47. The method of claim 44 wherein the crystallizing agent is silicon nuclei.
48. The method of claim 47
wherein conversion of the first amorphous layer to hemispherical grains before
formation of the second layer is substantially prevented and
wherein the first and second amorphous layers are crystallized to form the
polysilicon layer after the annealing step.
49. The method of claim 44 further comprising forming a plurality of memory cells in the
polysilicon layer, wherein portions of the cells comprise portions of the polysilicon
layer.
50. A method for controlling grain density in crystallized silicon, the method comprising:
forming an amorphous silicon layer on a wafer;
exposing the amorphous silicon layer to laser energy to create symmetrically
distributed nucleation sites; and
annealing the wafer,
wherein substantially no amorphous silicon remains between silicon grains after
the annealing step is complete.
51. The method of claim 50 wherein the amorphous layer is converted to polysilicon, and
further comprising forming a plurality of memory cells, wherein portions of the
memory cells comprise portions of the polysilicon.
52. The method of claim 50 wherein the plurality of memory cells comprise portions of a
monolithic three dimensional memory array.
53. A monolithic three dimensional memory array comprising memory cells comprising
polysilicon formed by a method comprising:
forming a first amorphous silicon layer on a wafer;

selectively introducing a crystallizing agent at nucleation sites at substantially uniform intervals on the first amorphous silicon layer;
annealing the wafer to grow silicon grains; and
forming the memory array, wherein the memory array comprises at least two levels of memory cells, one level formed vertically above another,
and wherein, after formation of the memory array, substantially no amorphous silicon remains between the grains.

54. A method for producing a wafer having a crystallized silicon layer with controlled defect density, the method comprising:
forming a first layer of amorphous silicon on the wafer;
selectively introducing a crystallizing agent on the amorphous silicon layer in a substantially symmetric pattern across a seeded area, the seeded area having a first distance between nucleation sites; and
annealing the amorphous silicon layer, wherein, after the annealing step, in the seeded area, a chance that a square area having a side less than about one fourth of the first distance has no more than one grain boundary is greater than about .75.
55. The method of claim 54 wherein the symmetric pattern is substantially evenly spaced in two dimensions.
56. The method of claim 54 wherein the crystallizing agent is silicon nuclei.
57. The method of claim 56 further comprising, before the annealing step, forming a second layer of amorphous silicon on and in contact with at least portions of the first amorphous silicon layer.
58. The method of claim 54 wherein the crystallizing agent is germanium.

59. The method of claim 58 further comprising, before the annealing step, forming a second layer of amorphous silicon on and in contact with at least portions of the first amorphous silicon layer.
60. The method of claim 54 wherein the crystallizing agent is laser energy.
61. The method of claim 54 wherein a monolithic three dimensional memory array comprising charge storage devices is fabricated on the wafer, portions of the devices comprising portions of the crystallized silicon layer.
62. A method for controlling grain boundaries in a polysilicon layer, the method comprising:
- forming a first amorphous silicon layer on a wafer;
 - forming a mask layer on and in contact with the first amorphous silicon layer;
 - etching the mask layer wherein portions of the amorphous silicon layer are exposed;
 - depositing silicon nuclei on the mask layer and on the first amorphous silicon layer;
 - forming a second amorphous silicon layer in contact with at least portions of the first amorphous silicon layer, and
 - annealing the wafer.